Technical Update
#2 2016

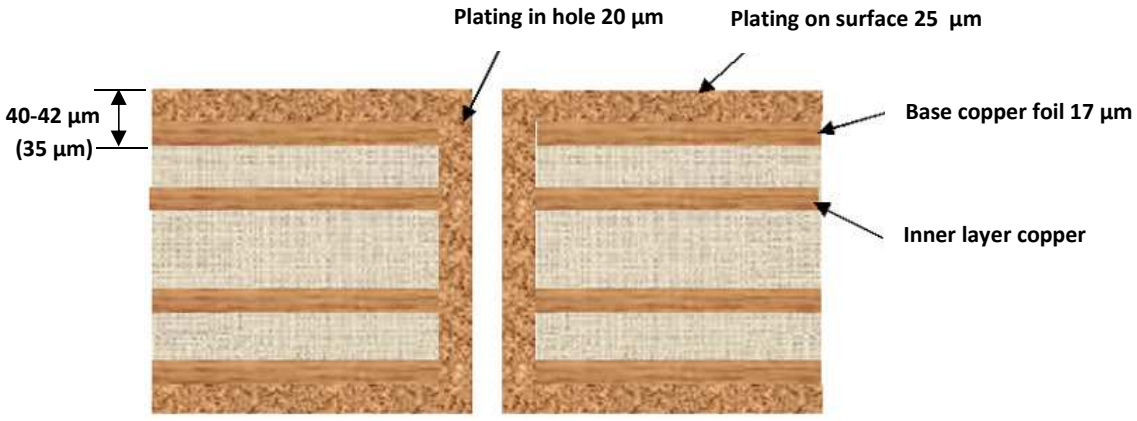
Copper thickness – specification & reality

In most cases the printed circuit copper thickness is not very crucial for the design, however it can be critical when impedance control, high currents or narrow tracks is involved.

Copper thickness on outer layer

The printed circuit board outer layer copper is built up by plating on a base copper foil. The plating-process add copper inside the vias and connects inner layer with outer layer. Specificed 35 µm copper thickness on outer layer starts with 17 µm base copper foil. Copper is plated on top of this foil and the plated copper thickness is determined by how much copper is required inside the viaholes. 20 µm copper plating is required for IPC class 2, total thickness will be 17+20=37 µm, in theory…
I reality we will end up with even higher thickness, as we have to consider:

- Copper foil manufacturing tolerances
- Treatment of the foil during processing
- Plating variations



Variations in the plating will affect final copper thickness more than all other parameters. Copper thickness on the pcb surface will always be higher than inside the holes and pattern distribution (layout) combined with variations in the electrolytical plating process, will cause local variations over the whole pcb surface. An even copper distribution will generate a smoother plating surface.
Specified 35 µm copper on outer layer will normally end up in 40-42 µm in practice (IPC class 2)

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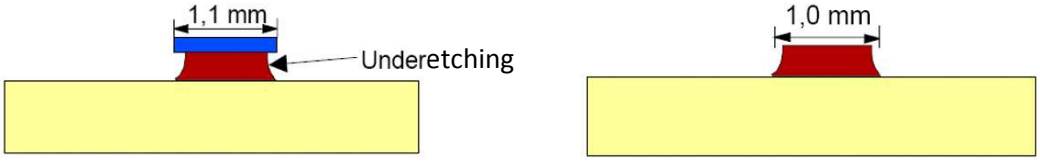
Copper thickness on inner layer

Inner layer will not pass any plating process as you use only base copper foil. That is why you always can calculate with lower copper thickness on inner layer compared to what is specified. Beside the copper foil manufacturing tolerance, the printed circuit processing will shave off some few µm. Specified copper thickness 35 µm will normally by 30-32 µm in practice. Specified copper thickness 70 µm will be 62-65 µm in practice.

These copper thicknesses has been measured in cross sections in practice. IPC allows even thinner copper on innerlayer. Read more about minimum values for copper thickness on inner and outer layer according to IPC-A-600, table 3-1, 3-2

Under etching and narrow tracks

Under etching is a well known phenomena always appearing during manufacturing of conductive pattern. The etching process removes copper both in depth and sideways due to the chemical wet process. The under etching is difficult to control, besides etch compensation made by the pcb manufacturer, so the base of the track will always be wider than the top.



The under etch effect means in practice that a combination of narrow tracks and thick copper is a bad idea, as the etching will have longer time to remove copper sideways due to the thickness. A track and gap of 0,1 mm is based on maximum 35 µm copper thickness. With increased copper thickness we will need to increase track and gap as well.

Copper thickness Specified	Absolute minimum Track/Gap	Recommended min. Track/Gap
35 µm	0,1 mm	0,15 mm
70 µm	0,2 mm	0,3 mm
105 µm	0,25 mm	0,35 mm
140 µm	0,3 mm	0,4 mm